Development of an Opensource, Openhardware, Software-Defined Radio Platform for Two-Way Satellite Time and Frequency Transfer

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***Abstract*—We describe an opensource, openhardware experimental Software-Defined Radio setup for prototyping various digital communication over microwave links with a geostationary satellite for assessing the impact of the various parameters on a Two-Way Satellite Time and Frequency Transfer link. Results consistent with the proprietary SATRE modem are demonstrated, including sub-ns resolution on ranging and two-way measurements. The emitted signal structure and impact of code length are assessed, and the signal acquisition and processing are described.**

***Index Terms*—SDR, TWSTFT, VSAT, PRN code, Time delay**

I. Introduction

Two-Way Satellite Time and Frequency Transfer (TWSTFT) is currently used for the computation of the Coordinated Universal Time (UTC) by direct comparison between atomic clocks disseminated worldwide. The classical means of spectrum spreading by introducing a pseudo-random noise (PRN) binary sequence modulating, using binary phase shift keying (BPSK), of a carrier is used to transfer time information, with the PRN generator being clocked by the reference frequency and triggered by a one pulse per second (1-PPS) signal.

While the historical development of the TWSTFT modem, initially the academic project of MITREX then the SATRE instrument sold by TimeTech GmbH, goes back to the 1980s, hardly any published reference [1]–[3] justifies the selected PRN pattern and the technological limitations at the time that might have driven some of the scientific decision whose relevance to current computational power might be questionable.

With the advent of Software-Defined Radio (SDR) solution, as demonstrated for the computation of UTC in [4], prototyping various codes, code lengths, or modulation schemes has become a matter of reprogramming a Field Programmable Gate Array (FPGA) matrix of logic gates, while recording the raw IQ stream of received signal allows for prototyping multiple processing algorithms on a given dataset. This technology has become available for the development of a TWSTFT prototyping framework thanks to

1) large storage capacity despite the data rates involved with SDR: at a sampling rate of 5 MHz and two channels recorded as 16-bit integer complex values, a data rate of 2.4 Gbytes/min is produced
2) large FPGA capacity on opensource and openhardware SDR platforms allowing to add PRN generation next to the data handling logic
3) efficient FPGA programming frameworks for efficient prototyping of novel modulation schemes and PRN sequences, in our case the Python-derived Amaranth framework.

In this article, we address the technical implementation of an SDR emitter complying with satellite service provider requirements, emitting the standard 70 MHz Intermediate Frequency (IF) signal feeding the upconverter of the Very Small Aperture Terminal (VSAT) transmitter (14 GHz) solely relying on an FPGA and output bandpass filter. We follow with the implementation of an SDR receiver relying on a dual channel radiofrequency frontend, either as Ettus Research B210 (at LNE-LTFB) with the AD9361 providing the local oscillator and variable gain amplifiers, or the Ettus Research X310 (at LNE-SYRTE). Finally, the signal processing steps for computing the relevant link indicators such as frequency translation offset of the downlink frequency (11 GHz) introduced by the satellite transponder, Signal to Noise Ratio (SNR) and most relevant time delay in ranging and two-way transfer are discussed. We conclude with a link demonstration between LNE-SYRTE (OP) in Paris and LNE-LTFB (LTFB) in Besançon.

II. Hardware architecture

SDR aims at restricting to a minimum the hardware implementation to move as much processing as possible to the software level. The setups used at OP and LTFB differ in their detailed implementation but share the common strategy of clocking the FPGA with metrological signals to generate the modulated 70 MHz IF, with a SAW-filtered split output feeding the VSAT upconverter on the one hand and a local reference channel of the coherent dual-channel SDR receiver on the other hand. On the receiver side, the second coherent channel is fed by the VSAT downconverter, hence providing a common timing reference between the locally generated signal and the signal received from the remote transmitter. While the receiver might not require a metrological reference

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since the common mode will be rejected during the differential measurement, our setup does clock the SDR receiver with metrological frequency references. At OP, the coherent dual-frequency receiver is an Ettus Research X310 fitted with two BasicRX boards, with the same FPGA in charge of generating the PRN code and the BPSK modulated IF carrier (Fig. 1). In order to reduce the lengthy synthesis duration during the prototyping state, the emitting FPGA at LTFB is separate from the receiver Ettus Research B210 SDR platform, although the latter board FPGA has been demonstrated to be suitable to also generate the transmitted signal. All software – using the RFNoC framework for the X310, a custom modification of the official gateware for the B210 or dedicated gateware for the external FPGA – is implemented in the Amaranth platform independent language.

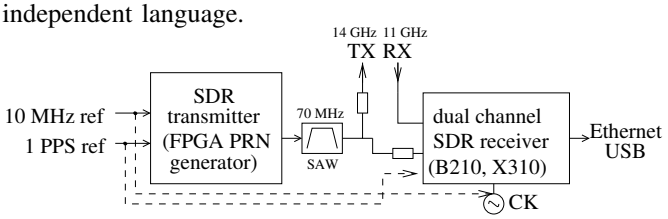

Fig. 1. General hardware architecture with an FPGA-based IF transmitter and a coherent dual-channel SDR receiver for recording the data to be post-processed.

III. Emitter: coding scheme

The emitted signal is synthesized by an FPGA clocked by the metrological 10 MHz and 1-PPS references, the only means with discrete logic to meet the stringent requirements of aligning the PRN code with the reference frequency and time signals. The design is portable to any FPGA fitted with a PLL fast enough to define the 70 MHz IF carrier BPSK modulated: in the case of the Zynq processor fitted on the Zedboard or the Spartan6 and Kintex7 FPGA fitted on B210 and X310 respectively, a core clock of 280 MHz is selected as an integer multiplication of the reference 10 MHz readily divided to generate the 70 MHz IF and the four states (00, 01, 11 and 00) of the QPSK modulation.

While SDR provides a generic and flexible radiofrequency interface, emission is plagued by spurious spectral components produced by the digital synthesis: here. the 70 MHz is produced as a square wave as a General Purpose Input/Output (GPIO) interface of the FPGA associated with numerous overtones and unwanted spectral components. Dedicated 70 MHz Surface Acoustic Wave (SAW) filters are selected as C-TECH 321823 or SAWTEK 851547 for keeping the signal within the 4-MHz wide currently allocated satellite transponder band and reject by over 50 dB out-of-band spectral components. The high losses of these filters does not impact the link budget since the digital GPIO voltages must be attenuated anyway to match the SATRE modem output power (typically -20 dBm range) feeding the VSAT upconverter.

IV. Receiver: signal processing

On the receiver side, a single board or laptop computer fetches samples from a dual channel SDR receiver, with one channel acting as reference through a loopback link from the emitter and the second channel connected to the VSAT downconverter.

Unlike the closed Costas loop classically used for real time frequency tracking of the BPSK signal, in the context of SDR post-processing the identification of the frequency offset between nominal carrier frequency and received signal frequency is achieved by squaring to cancel BPSK spectrum spreading and identifying the spectral component at twice the frequency offset. A numerically controlled oscillator compensates for the frequency offset before correlating with the local copy of the code. A classical improvement on the time resolution of the correlation peak is brought by parabolic fitting, improving the delay resolution by a factor equal to the SNR on the correlation peak.

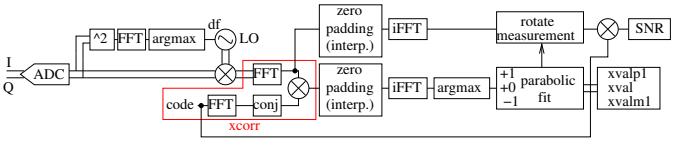

Fig. 2. Signal processing scheme on the receiver for extracting the coarse frequency offset through the Fourier transform of the squared signal, cross-correlating in the Fourier domain to benefit from oversampling by zero-padding, identifying the cross-correlation maximum and polynomial fit for improving delay resolution, and alignment of the code with the received signal for power and hence signal to noise ratio estimate.

Under such considerations, the tradeoff lies between selecting a short PRN code leading to lower Pulse Compression Ratio (PCR) SNR improvement during the correlation but allowing for averaging multiple successive delay estimates, or a long code with fewer estimates for averaging but improved PCR. In order to avoid the ranging and two-way transfer uncertainty related to a short Pulse Repetition Interval (PRI) induced by a short code, a PRN length of at least the two-way trip of 270 ms is selected, and 1-s long code appears as best suited to avoid introducing additional coding schemes for determining the correlation peak associated with the 1-PPS of the beginning of the second.

V. Results

The IF signal is generated by an FPGA clocked by the metrological source, as well as the VSAT upconverter, but the satellite transponder induces uncontrolled frequency offset called satellite frequency translation. In our processing scheme, each second of data is analyzed through a Fourier transform of the squared signal to collapse the frequency spreading by removing the BPSK modulation and hence identify with sub-0.5 Hz resolution the frequency offset. During multiple day recording sessions, the diurnal frequency fluctuation is clearly observed (Fig. 3) but does not impact the code-delay measurement other than through a signal to noise ratio degradation if the frequency offset remains excessive.

Correlating the 2.5 Mchips-long PRN code sampled at 5 MS/s introduces artefacts as the satellite is moving at a rate of a few nanoseconds/s depending on the orbital parameters. For example at a rate of 3.2 ns/s and a sampling period

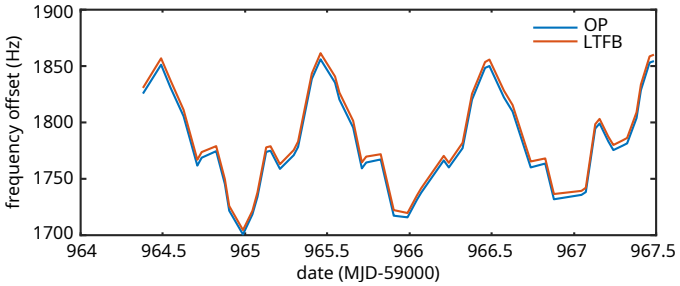

Fig. 3. Frequency offset observed every hour during TWSTFT sessions between OP and LTFB: both stations observe the same offset, hinting at the satellite transponder as the source of the frequency translation between uplink and downlink signals.

of 200 ns, correlation peak position fluctuations of a few nanoseconds are observed every 62.5 s (Fig. 4), inducing unwanted excessive standard deviations on the measurements sessions lasting 180 s. This session duration is derived from the 8 GB broadband Random Access Memory (RAM) used for storing the datastream on the single board Raspberry Pi4 computer used in the current implementation.

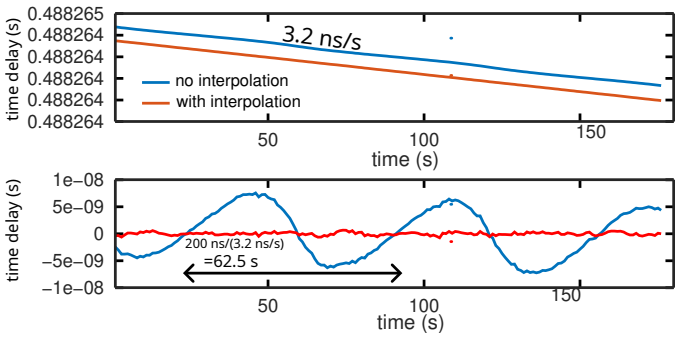

Fig. 4. Top: ranging time delay over a 3-min. session, and bottom after removal of the parabolic trend. Top without oversampling (5 MS/s), bottom at 15 MS/s by interpolating using zero-padding prior to inverse Fourier transform when computing the correlation in the Fourier domain.

The cause of this periodic fluctuation of the cross-correlation peak fine positioning with sub-sampling period resolution is attributed to the parabolic fit performed on the cross-correlation peak magnitude and its two neighbors: as shown on Fig. 5, the cross-correlation peak slowly shifts from a sampling point to the middle between two sampling points and back to a sampling point, leading to a loss of signal to noise ratio of the polynomial fit and offset induced by the non-parabolic shape of the correlation peak. Oversampling in the Fourier domain by zero-padding the product of the signal and code Fourier transforms prior to inverse Fourier transform to recover the time-domain correlation solves the issue by adding preliminary a $sinc()$ fit to the correlation peak shape.

This issue is solved by oversampling the received signal: since computing the correlation is most efficiently achieved by computing the Fourier transform of the code (pre-processing) and the received signal whose complex conjugate is multiplied with the former prior to inverse Fourier transform, efficient oversampling is implemented by zero-padding the Fourier transform product prior to the inverse Fourier transform. Such a procedure cancels the unwanted delay fluctuations and

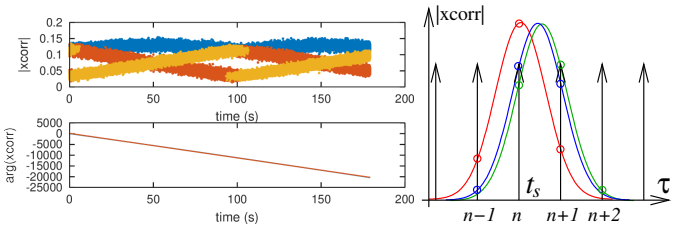

Fig. 5. Left: top, evolution of the cross-correlation magnitude peak (blue) and its two neighbors (red, orange) during a 3-minute long acquisition as the satellite is moving (middle) as shown in the fine delay analysis.

provides typical sub-ns standard deviation on the measured ranging or two-way delays over 3-min. sessions as determined by the available broadband storage resources (Fig. 6).

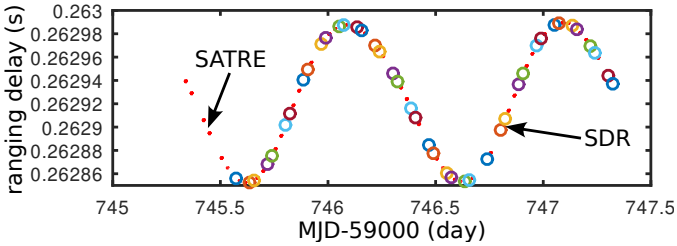

Fig. 6. Ranging measurement over 36 h using the SDR setup (circles) during odd UTC hours and the SATRE modem (dots) during the even UTC hours.

Finally, SNR is a core indicator of link budget: computing the SNR is achieved by assessing the signal power as the integral of the product of the aligned PRN sequence with the received signal, while the noise is given by the standard deviation of the received signal. Fig. 7 illustrates the evolution of the power component of the SNR calculation,

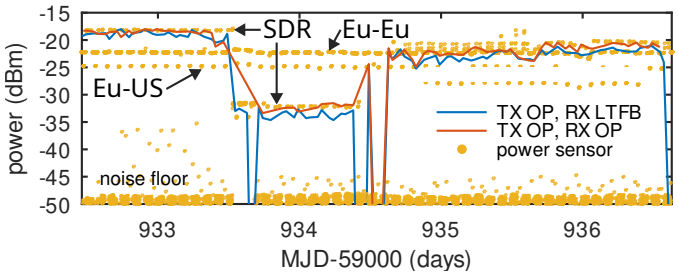

Fig. 7. Signal power: in yellow the output of a power sensor located at the input port of the transmitting VSAT parabola at OP, in red the ranging signal power recorded at OP and in blue the power of the signal transmitted by OP and received by LTFB. Beyond the consistency of the measurement, the transmitted power drop by 10 dB during MJD 59934 is well visible in all curves, demonstrating the accuracy of the SDR calculation.

As a result of these analysis, the remaining degree of freedom is the PRN code length. A long code improves the SNR thanks to the long integration duration of the correlation, but reduces the number of estimates of time transfer during a one second duration. A short code reduces each estimate SNR but allows for averaging multiple estimates. Since the correlation of a known PRN code of length N with the received signal improves the SNR as $\sqrt{N}$ on the one hand,

and on the other hand averaging during a one-second period also improves the SNR by $\sqrt{N}$, the resulting Allan deviation is expected to be independent on code length. This result is verified experimentally in a ranging measurement lasting each 3-min with varying code lengths as illustrated in Fig. 8: the Allan deviation is in the 200 ps range at 1 s integration time for all code lengths. Hence, the selection of the code length is not driven by SNR considerations but by additional requirements, e.g. packing a number of digital bits over the PRN as discussed in the next section, with shorter PRN codes allowing for higher communication bitrates.

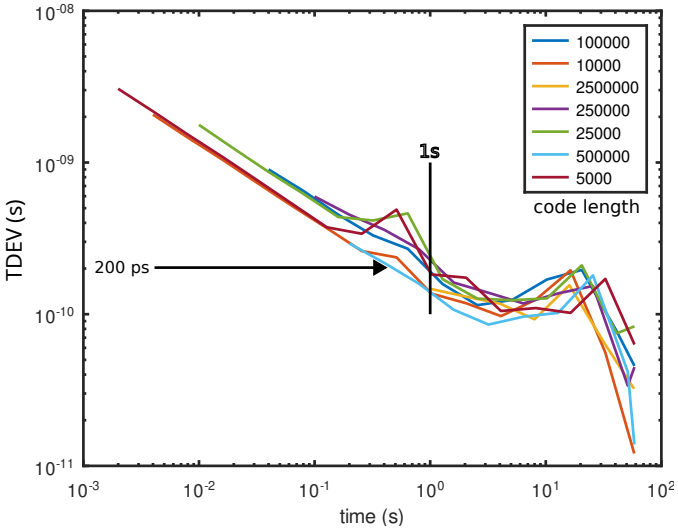

Fig. 8. Allan time deviation of the ranging measurement as a function of code length.

VI. Timing Requirements

TWSTFT assumes that the common impact of the satellite distance and motion is compensated for by simultaneously analyzing the signal transmitted from one end and received by the other hand. The assumption that the same sentence transmitted at the same time at both ends of the link will be compared requires some timing requirements between the two receivers. Since the remote measurement sites can hardly be synchronized accurately, embedding the coarse timing signal (1-PPS counter) in the transmitted message provides the means for making sure the local code is compared with the remote signal received at the same time. Adding this binary message is performed by XORing the PRN sequence with the transmitted message – at first a counter since the beginning of the transmission – to help synchronize the messages at both ends. However, XORing the PRN sequences induces a new challenge of aligning the local copy of the PRN with the received signal since the cyclicity assumption of the correlation in the Fourier domain is lost when flipping the bit state. Hence, adding the digital coding scheme requires not only detecting the correlation peak and monitoring its position but tracking the PRN and aligning with the received signal as classically done in the GPS or SATRE Delay Locked Loop (DLL) control (Fig. 9). Alternatively, the digital code is recovered by subtracting the phase of the squared BPSK signal from the received signal to remove the phase drift and only analyze the π dependent phase shift representative of transmitted bit state.

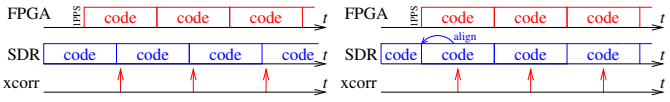

Fig. 9. Left: openloop measurement of the correlation peak position, assuming the cyclicity of the code during the correlation. Right: tracking the correlation peak to make sure the local copy of the PRN is aligned with the received signal and hence avoid the correlation loss when the bit state is flipped by the digital message communication.

In order to analyze the impact of comparing codes transmitted a different times between the two remote stations, Fig. 10 models the time offset induced by a 1-s (blue) or 2-s (red) error on the code comparison, considering a diurnal position fluctuation of the satellite inducing a ± 75 μs ranging delay variation: although the residual is well below the sampling period of 200 ns, the impact is above the targeted ± 100 ps variation from measurement to measurement of the TWSTFT delay comparison. This result emphasizes the need to encode the transmit time as a digital layer on top of the PRN sequence, most easily introduced by XORing the transmitted time code with the PRN priori to BPSK modulation of the IF carrier.

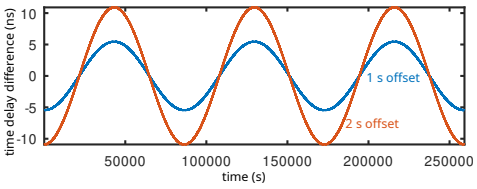

Fig. 10. TWSTFT delay induced by a 1-s (blue) or 2-s (red) error on the time at which the code was transmitted by one station and analyzed by the remote one.

VII. Conclusion

We have demonstrated a functional SDR-based TWSTFT framework for analyzing the various parameters of the digital communication. All software for reproducing the proposed setup is available at https://github.com/oscimp/amaranth_twstft

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